REMARKS

Claim rejections under 35 USC 103

Claims 1-18 have been rejected under 35 USC 103(a) as being unpatentable over Weber (6,631,448) in view of Steely (2005/0160430). Applicant respectfully traverses this rejection. Claim 1 is discussed as representative of all the pending claims in this respect, insofar as the following limitation is concerned. This limitation, as amended, is that the logic determines whether *a cache miss* relating to a memory unit should be transmitted *only* to a sub-plurality of nodes, where this sub-plurality of nodes are in number less than the plurality of nodes but greater than one. That is, when you have a cache miss in the claimed invention, this cache miss is transmitted *only* to a sub-plurality of nodes – not all the nodes, and not just one of the nodes.

In the previous office action response, Applicant argued this limitation, minus the added modifier "only." In response, the Examiner stated that the claim language fails to explicitly define transmitting a cache miss to *only* a sub-plurality of nodes greater than one and less than all the plurality of nodes. (See final office action, p. 7, para. 4.) Therefore, in response, Applicant has added this limitation to the independent claims. Support for this amendment is found in the patent application as filed at least in FIG. 2, parts 204 and 206, and in FIG. 6, parts 608 and 610. In FIGs. 2 and 6, if the determination of parts 204/608 is successful, then the cache miss is *only* transmitted to the sub-plurality of nodes in parts 206/610 (i.e., the cache miss is *never* transmitted to all the nodes). This is because the methods of FIGs. 2 and 6 are described as transmitting a cache miss to all the nodes in parts 208/614 only if the determination in parts 204/608 is *un*successful. Therefore, if the determination in parts 204/608 is successful, then the cache miss is never transmitted to all the nodes (i.e., parts 208/614 are never performed in this case), and it can be said that the patent as filed at least in this way supports the claim limitation that the cache miss is only transmitted to the sub-plurality of nodes in parts 206/610.

Applicant respectfully submits that Weber in view of Steely does not teach, disclose, or suggest this limitation of the claimed invention. In Weber in view of Steely, a cache miss is either sent to a single node, as in column 6, lines 11-34 of Weber, [1] or to "one or more" nodes, as in

[1] This excerpt of Weber reads as follows:

> If processor 1941 does not find the data in cache 1942 (a "cache miss"), the processor issues a request onto P6 memory bus 230 for the data. The bus request includes the real address of memory line 1900 and the identification of home node 1920 for memory line 1900. **If memory line 1900 resides on a different node, MCU 1943 (130) of local node 1940 generates a network request for the cache line 1900 across Interconnect 110 to home node 1920.**

Thus, for a cache miss in Weber, you only transmit the cache miss (i.e., the network request) to the home node, which, of course, is just *one node*. By comparison, in the claimed invention, you transmit the cache miss to a number of nodes that is *greater than one* but less than all the nodes.

Applicant further notes that in the final office action, the Examiner has stated that Weber in the context of Weber in view of Steely teaches transmission of a cache miss to a sub-plurality of nodes lesser in number than all the plurality of nodes, in column 5, line 55, through column 6, line 6. (See final office action, p. 7, para. 4.) However, Applicant notes that this particular excerpt of Weber does not have anything to do with transmission of a *cache miss*, and therefore cannot be considered under the broadest reasonable interpretation thereof as teaching, disclosing, or suggesting this aspect of the claimed invention. Indeed, the word "miss" is not present in this excerpt of Weber. It appears that this excerpt of Weber is completely related to selective transmission in the context of *invalidation*, which is different than selective transmission in the context of a cache miss. (In the latter, a given node communicates with one or more other nodes when its cache does not have the memory line in question; in the former, a given node communicates with one or more other nodes when it wants to invalidate the memory line in question at the caches of these other nodes – a very different situation.) Thus, Applicant submits

paragraphs [0054]-[0056] of Steely.[2] Thus, whereas the claimed invention is limited to transmitting a cache miss to a sub-plurality of nodes that in number is *greater than one* but *less than the entire number of nodes*, in Weber in view of Steely, *at best* you transmit a cache miss to *one or more nodes*. That is, in the claimed invention the lower "limit" of nodes to which you transmit a cache miss to is *greater than one*, whereas in Weber in view of Steely the lower "limit" of nodes to which you transmit a cache miss to is *just one node* (since transmitting a cache miss to "one or more nodes" means that you can transmit a cache miss to just one node, which is encompassed by the phrase "one or more nodes"). Likewise, in the claimed invention the upper "limit" of nodes to which you transmit a cache miss to is *less than the total number of nodes*, whereas in Weber in view of Steely the upper "limit" of nodes to which you transmit a cache miss to is *all the nodes* (since transmitting a cache miss to "one or more nodes" means that you can transmit a cache miss to *all* the nodes, which is encompassed by the phrase "one or more nodes").

To make this even clearer, consider the following example. You have *N* total nodes, and you submit a cache miss to *x* of these nodes. In the claimed invention, $1 < x < N$. In Weber in view of Steely, $1 <= x <= N$. Thus, the difference between the claimed invention and Weber in

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that Weber at best teaches, discloses, and suggests that a cache miss is transmitted to only a single node, as described in the previous paragraph.

[2] This excerpt of Steely states the following:

> In response to a cache miss on a desired cache line, a processor (e.g., 117) searches its associated owner predictor (e.g., 165) for an entry corresponding to the desired cache line. If an entry is found, the processor 117 selects the indicated owner processor as a speculated target processor for a request for the desired cache line. **If no entry is found corresponding to the desired cache line, one or more default processors can be selected.**

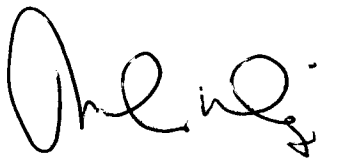
Thus, for a cache miss in Steely, *at best* you only transmit the cache miss to *one or more nodes*. By comparison, in the claimed invention, you transmit the cache miss to a number of nodes that is *greater than one* but less than all the nodes.

view of Steely is that the first mathematical operator "<" (i.e., less than) is replaced by the mathematical operator "<=" (i.e., less than or equal to) in Weber in view of Steely, and the second mathematical operator "<" is also replaced by the mathematical operator "<=" in Weber in view of Steely. Where the claimed invention is limited to "1 < x < N," and Weber in view of Steely at best teaches "1 <= x <= N," it cannot be said that Weber in view of Steely suggests, teaches, or discloses all limitations of the claimed invention. Therefore, Weber in view of Steely does not render the claimed invention *prima facie* obvious or unpatentable.

Conclusion

Applicants have made a diligent effort to place the pending claims in condition for allowance, and request that they so be allowed. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Mike Dryja, Applicant's representative, at 425-427-5094, so that such issues may be resolved as expeditiously as possible. For the reasons discussed above, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,



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Michael A. Dryja, Reg. No. 39,662
Attorney/Agent for Applicant(s)

Law Offices of Michael Dryja
1474 N Cooper Rd #105-248
Gilbert, AZ 85233
tel: 425-427-5094
fax: 206-374-2819